Claims

What is claimed is:

1. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus comprising:

a FIFO random access memory (RAM) having a data input for receiving data and control information and a data output for outputting said data and control information; said FIFO RAM including a plurality of locations for storing a plurality of words, each word including a set number of bits;

write clocked logic for loading said data and control information to said FIFO RAM at a first clock frequency;

asynchronous read clocked logic for outputting said data and control information from said FIFO RAM at a second clock frequency; and

said first clock frequency of said write clocked logic and said second clock frequency of said asynchronous read clocked logic and a data width of said FIFO RAM being selectively provided for outputting said data and control information from said FIFO RAM with no back pressure.

2. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 1 wherein said FIFO RAM includes a multiple location FIFO RAM used on each asynchronous boundary.

3. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 1 wherein loading said data and control information enables predefined higher level functions including interleaving multiple direct memory accesses (DMAs), and providing an abort and discard data function.

4. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 1 wherein said data and control information includes a data field storing data being direct memory accessed (DMAed) through said FIFO RAM.

5. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 1 wherein said data and control information includes a control field storing parity or error correction code (ECC) control information.

6. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 1 wherein said data and control information includes a control field storing buffer address control information for writing a data field to a buffer of a target engine.

7. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 1 wherein said data and control information includes a control field storing byte valid control information for writing a data byte from a data field to a buffer of a target engine.

8. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 1 wherein said data and control information includes a control field storing engine select control information for selecting a target engine.

9. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 1 wherein said data and control information includes a control field storing buffer select control information for selecting a buffer on a target engine.

10. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 1 wherein said data and control information includes a control field storing authorization code control information for discarding said data and control information being outputted from said FIFO RAM.

11. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 1 wherein said write clocked logic for loading said data and control information to said FIFO RAM at said first clock frequency includes a Gray code increment block encoding a write address input to said FIFO RAM.

12. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 11 includes a multiplexer coupled to said Gray code increment block and receiving a write strobe select input for incrementing a Gray code write address.

13. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 12 includes a pair of synchronization latches to provide a synchronization input to said asynchronous read clocked logic for outputting said data and control information from said FIFO RAM at said second clock frequency.

14. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 13 wherein said asynchronous read clocked logic for outputting said data and control information from said FIFO RAM at said second clock frequency includes a Gray code increment block encoding a read address input to said FIFO RAM.

15. A flow through asynchronous elastic first-in, first-out (FIFO) apparatus as recited in claim 13 wherein said asynchronous read clocked logic includes a multiplexer coupled to said Gray code increment block encoding said read address input to said FIFO RAM and receiving a valid strobe select input for incrementing a Gray code read address.

16. A method for implementing multi-engine parsing and authentication with a flow through asynchronous elastic first-in, first-out (FIFO) apparatus including a FIFO random access memory (RAM) having a data input for receiving data and a data output for outputting said data; the FIFO RAM including a plurality of locations for storing a plurality of words, each word including a set number of bits; said method comprising the steps of:

loading data and control information to the FIFO RAM at a first clock frequency;

outputting said data and control information from the FIFO RAM at a second clock frequency; and

selectively providing said first clock frequency and said second clock frequency and a data width of the FIFO RAM for outputting said data and control information from the FIFO RAM with no back pressure.

17. A method as recited in claim 16 wherein the step of loading data and control information includes the steps of storing a data field and a plurality of control fields in the FIFO RAM.

18. A method as recited in claim 17 wherein the steps of storing said plurality of control fields including storing an engine select control field for selecting a target engine.

19. A method as recited in claim 17 wherein the steps of storing said plurality of control fields including storing an authorization code control field for discarding said data and control information being outputted from the FIFO RAM.

20. A method as recited in claim 17 wherein the steps of storing said plurality of control fields including storing an address control field for writing a data field to a buffer of a target engine.

21. A method as recited in claim 17 wherein the steps of storing said plurality of control fields including storing a byte valid control field for writing a data byte from a data field to a buffer of a target engine.

22. A method as recited in claim 17 wherein the steps of storing said plurality of control fields including storing a buffer select control field for selecting a buffer of a target engine.

23. A method as recited in claim 17 wherein the steps of storing said plurality of control fields including storing a parity or error correction code (ECC) control field for providing parity of ECC protection.